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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,343	01/24/2002	Debashis Bhattacharya	162.7513USU	8030

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EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,343	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- Th MAILING DATE of this communication appears on the cov r sh et with the corr spondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003 and 09 December 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner. draftsperson

10)☒ The drawing(s) filed on *24 January 2002* is/are: a)☐ accepted or b)☒ objected to by the ~~Examiner~~.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed on 10/15/2003 and IDS filed on 12/9/2002. Claims 1-22 are pending, wherein claims 1,6-8,13-14,19-20,22 have been amended. Claims 1-22 have been examined. Applicant's arguments are not persuasive; therefore, the previous Office Action is incorporated herein.

Drawings

2. The drawings (containing Figs. 1, 1a) were received on 10/15/2003. These drawings are approved by the Examiner.

3. As indicated in the previous Office Action, the drawings filed on 1/24/2002 are acceptable subject to correction of the informalities noted above and indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-3,12,13,17--22** are rejected under 35 U.S.C. 102(e) as being anticipated by **Cirit** (US Patent No. 6,523,156).

Cirit discloses an apparatus and methods for generating an integrated circuit layout design in which the circuit netlist is optimized using equivalent cell replacement (abstract; Fig. 1).

As per **claims 1,2,20,22**, all of the elements of the claims are illustrated in Fig. 3 (see also col. 7, line 43 to col. 12, line 47), wherein the functional description is provided as part of step 102 (see also col. 7, lines 45-65), the design constraints load, power, timing, delay constraints associated with cell replacement operations (blocks 306-314), which are related to context-of-use in the sense that depending on the particular circuit path and its requirement, a particular cell library implementation selected, and wherein the storage medium for storing such instructional steps are also described in col. 4, lines 18-31.

As per **claim 3**, the determination of matching existing cell is also described in col. 8, line 13 to col. 9, line 28.

As per **claims 12-13**, the further step of characterizing the cell based on the constraints is also part of the steps 306-314, having constraints associated the various characterization/evaluation for cell replacement operations, including regions of cells (i.e., cells within the timing path evaluated--col. 9, lines 4-7).

6. As per **claims 17,18,19,21**, the characterization being done at the transistor level, partitioned to realize the at least one standard cell, formed on the region, and/or comply with a standard cell design flow is also described in col. 7, line 45 to col. 8, line

12, wherein the partitioning of the circuit designs is further described in col. 3, lines 25-47 in which the circuit is grouped and mapped as part of the synthesis (304) of Fig. 3, described in col. 7, line 43 to col. 8, line 12) wherein such application to transistor level partitioning or grouping is further described in col. 12, lines 12-27.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 4-11,14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Cirit** (US Patent No. 6,523,156) in view of **Touzet** (US Patent No. 6,519,609).

As per **claims 4,5,8,9**, **Cirit** disclose all of the elements of claim 3, which the claims respectively depend, as discussed previously. However, **Cirit** failed to particularly teach the use of signature determination, including evaluating to determine a possible match, and using the signature as part of the constraint, including timing constraint. **Touzet** teach the use of signature determination, including evaluating to determine a possible match as part of the logic synthesis to rapidly arrived at the desired circuit implementation (col. 2, line 43 to col. 3, line 67; col. 13, lines 33-41). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the use of signature determination into the system/method of **Cirit**

because such method would further provide rapid logic synthesis from high level description as taught by **Touzet** and further supported by **Cirit** for further context-of-use cells replacement (see **Cirit**, col. 7, line 43 to col. 8, line 12).

As per **claims 6-7,14-16**, **Cirit** disclose all of the elements of claims 1,12, which the claims respectively depend, as discussed previously. However, **Cirit** failed to particularly teach determining of at least one input permutation or one possible input complement (i.e., inversion) or vectors characterization. Such methods are taught by **Touzet** as part of the using signature for the logic synthesis from high level description (see col. 2, line 43 to col. 3, line 67). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the use of signature determination, that includes determining of at least one input permutation or one possible input complement (i.e., inversion) or vectors characterization, into the system/method of **Cirit** because such method would further provide rapid logic synthesis from high level description as taught by **Touzet** and further supported by **Cirit** for further context-of-use cells replacement (see **Cirit**, col. 7, line 43 to col. 8, line 12).

As per **claims 10-11**, **Cirit** in view of **Touzet** disclose all of the elements of claim 9, which the claim depends, as discussed above, wherein the further limitation that rise times and fall times are ordered and compared is also within the scope of **Cirit** in view of **Touzet** since **Cirit** also teaches sorted/ordered list of rise times and fall times for use in cells selection (col. 7, lines 1-26) and **Touzet** further make use of signature determination that incorporates timing constraint/cost function (col. 13, lines 33-41) as

discussed in the rejection of claim 9 above, for which the rise times and fall times of **Cirit** (i.e., timing constraint) is applicable for cell replacements.

Remarks

9. The objections of **claims 6-8,13,15,17-21** due to the noted informalities are withdrawn in light of Applicant's amendments to the claims which corrected these informalities.

10. As per **claims 1-2,12,13,17-22**, Applicant argued that the claims are patentable over **Cirit** (US Patent No. 6,523,156) because **Cirit** does not appear to be concerned with reduction in the number of cells for implementing the IC design as claimed but is directed to methods of timing optimization for design netlists, wherein an original cell is replaced with another cell from a family of cells having the same replacement delay as the original cell and further the choices for replacement cells are relatively large, but not reduced in number. The Examiner is not persuaded. Although the Examiner agrees that the method of **Cirit** use cell replacements, this reduction in the number of cells for implementation of the IC design is also part of the selection process. By using the functional specification and the design constraints in the context-of-use as discussed in the rejection above, the selection of the particular cells implementation are limited to or reduced to the particular cell implementation(s) which meet the design constraints (i.e., of all the implementations of the various cells stored in the cell library, only those which have the functionality required by the functional specification and meet the design constraints are considered for replacement; thus, the number of distinct IC logic cells for implementing the IC is reduced as part of the determining/mapping step).

11. As per **claim 3**, Applicant argued that matching step/mean disclosed by **Cirit** is not the same or equivalent to Applicant's claimed invention because Applicant's claimed matching as an equivalent/compatability of functionality and in addition to functionality, the target for matching is annotated with constraints that preferably relate to the target design's use in a design environment whereas **Cirit**'s matching clearly refers to a cell "electrically appropriate for the load at the output of the cell". The Examiner is not persuaded. First of all, **Cirit**'s matching first of all matches the functionality of the desired circuit to be replaced by matching to the particular cell family (i.e., a cell family is a group of cells with the same logic function but may have one or more different characteristics) (col. 8, lines 25-26) and then is matched to the design constraints (i.e., load and timing requirements), thus providing for both the equivalent functionality/compatibility as well as the constrained based design's use in the design environment (i.e., the particular design optimization).

12. As per **claims 17-21**, Applicant argued that **Cirit** failed to explicitly disclose the partitioning at the transistor level. The Examiner is not persuaded. First of all, the partitioning of the circuit designs is further described in col. 3, lines 25-47 in which the circuit is grouped and mapped as part of the synthesis (304) of Fig. 3, described in col. 7, line 43 to col. 8, line 12) wherein such application to transistor level partitioning or grouping is further described in col. 12, lines 12-27.

13. As per **claims 4-11,14-16**, Applicant argued that since **Cirit** failed to teach or suggest the all of the elements of claim 1, from which the claims depend, the claims are patentable over **Cirit** in view of **Touzet**. Since **Cirit** disloses all of the elements of

claim as given above, the further incorporation of the teachings of **Touzet** and the motivations for incorporating the teachings of **Touzet** as given above, are applicable to the claims and accordingly rendered the claims unpatentable over the prior arts made of record.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicants are requested to consider them carefully in response to this Office Action.

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 703-306-3039. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(703) 746-4111 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing)

Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

17. **Applicant should note that effective May 1, 2003, the United States Patent and Trademark Office has a new Commissioner for Patents address for**

transitioning to the new Office location in Alexandria, VA, wherein correspondence in patent-related matters to organizations reporting to the Commissioner for Patents must now be addressed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PK
December 27, 2003

VUTHE SIEK
PRIMARY EXAMINER